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Patent

Attorney Docket No. MTI-31267

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant (s)	:	Polinsky et al.
Serial No.	:	09/584,975
For	:	Modified Facet Etch to Prevent Blown Gate Oxide and Increase Etch Chamber Life
Filed	:	May 14, 2001
Examiner	:	Lynette T. Umez Eronini
Group Art Unit	:	1765
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CERTIFICATION UNDER 37 CFR 1.8(a) and 1.10

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Date: February 24, 2003

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RESPONSE UNDER 37 C.F.R. § 1.111

This response replies to the Office Action mailed February 4, 2003 (Paper No. 3).

The Examiner rejected Claims 1, 8-11, 16 and 19-21 under 35 U.S.C. § 112, second paragraph as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Specifically, the Examiner finds the meaning of the term "target depth" unclear. Additionally, the Examiner finds the term "predetermined" indefinite because it reads on a nebulous metal step conducted prior to manipulative steps of the claimed invention. The Applicant traverses these rejections as follows.

The term "target depth" is clear from the claims, is fully described in the specification and is a standard term of art. The claims clearly state that target depth is the depth at which the

inventive etching process is terminated. See preamble to Claim 1 and final step of each independent claim. Additionally, the term is used unambiguously to mean such throughout the specification. Moreover, the term "target depth" is a term of art found in the granted claims of other U.S. patents which, are of course, presumed to be valid with respect to all sections of the statute. As an example, attached are the Claims pages from USP 6,225,234 obtained off the USPTO database. The Examiner will note in Claim 1 the use of the term "target depth" in a manner identical to the manner of the current claims. As such, the Examiner's rejection is in error and should be withdrawn.

Likewise, the term "predetermined depth" is a standard term found in numerous U.S. patents. As examples, attached are the Claims pages for USP Nos. 6,518,624 and 6,511,777 which demonstrate the use of the term "predetermined depth" in a manner identical to the current claims. As such, the Examiner should reconsider and withdraw his rejections based on § 112, paragraph 1.

The Examiner rejected Claims 1-10 under 35 U.S.C. § 103(a) as being unpatentable over Doan (USP 5,346,585) in view of Laxman (USP 5,774,196) in view of Yao et al. (USP 5,814,564). The Examiner states that Doan teaches a method for facet etching a semiconductor device to a target depth. The Examiner admits that Doan fails to teach both that the first layer is formed to a thickness at least equal to the target depth and that the specified depth in which the first etch is terminated with respect to the target depth. The Examiner then relies on Laxman to demonstrate that the layer thickness is a results effective variable. The Examiner then also admits that Doan in view of Laxman fails to teach: terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth; etching the first layer in a second etch by contacting the first layer with a reactive chemical gas/plasma; and terminating the second etch when the first layer has been etched to the target depth. The Examiner then relies on Yao et al. for the teaching of a method of etching back an oxide layer by employing six etching steps. The Examiner states that "since each of these steps are performed in a specified time, then using Yao et al.'s steps of etching an oxide layer would inherently read on [the current claims]". The Applicants traverse on the grounds that the cited prior art fails to teach all elements of the invention and are not properly combinable.

Specifically, to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. MPEP §2143.03 (citing to *In re Royka*, 180 USPQ 580 (CCPA 1974)). Moreover, showing that the prior art can be combined or modified is not sufficient, of itself, to establish *prima facie* obviousness. See MPEP §2143.01. Nor can an obviousness rejection be supported merely by showing that it would be "obvious to try" the claimed invention. See, e.g., *In re Fine*, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Rather, in order to establish a *prima facie* case of obviousness, the Examiner must show some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. Furthermore, in leading one skilled in the art, the prior art must suggest to the ordinary skilled artisan that the combination should be carried out and would have a reasonable likelihood of success, viewed in the light of the prior art. *In re Dow Chemical Co*, 5 USPQ2d 1529, 1532 (Fed. Cir. 1988)(emphasis added). Indeed, both the suggestion and the expectation of success must be found in the prior art, not in the Applicant's disclosure. Id. More specifically, the Federal District Court of D.C., which has jurisdiction over the USPTO, recently ruled that the suggestion or motivation to modify or combine prior art must be explicit in the prior art. See *Winner Int'l. Royalty Corp. v. Wang*, 48 USPQ2d 1139 (DCDC 1998). Moreover, a prior art reference must be considered in its entirety with consideration given to disclosures that diverge or teach away from the invention at issue as well as disclosures which direct the skilled artisan to the invention. *Ashland Oil, Inc. v. Delta Resins & Refractories, Inc.*, 776 F.2d 281, 300 (Fed. Cir. 1985). The Applicants believe that the Examiner's § 103 rejections fail to meet the above standards.

First, as the Examiner has stated, Doan teaches facet etching a semiconductor device to a target depth. Thus, Doan does not teach terminating the first etch when the first layer has been etched to a predetermined depth which is less than the target depth. There is no disclosure or suggestion in Doan of terminating the etch prior to the target depth or using a two-stage etch. Indeed, for the purposes of Doan, terminating the facet edge prior to reaching the target depth would be unsuitable because the target depth would not then be reached. If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Moreover, a two stage etch, wherein

the second stage etch is done by contacting the first layer with a reactive chemical gas/plasma, is a different principle of operation from a one stage etch performed exclusively with a plasma beam as taught in Doan. As such, Doan fails to teach or suggest the current invention and may not be properly modified as proposed by the Examiner.

The Examiner's use of Laxman does not advance the proposed *prima facie* case. Indeed, the teaching of Laxman is irrelevant to the current invention. The teaching of Laxman, at best, may be interpreted to indicate that layer thickness is a result effective variable in some context but the teaching does not indicate that layer thickness is a result effective variable in the context of the current method of facet etching. While the thickness of an insulating layer may well affect the performance of a semiconductor device, the layer thickness does not affect the performance of the current method. In other words, one skilled in the art would not change the thickness of a layer expecting to improve or alter the performance of the current method. Rather, the operational parameters of the current method would be optimized for different layer thicknesses. Moreover, even if Laxman did render the thickness of the first layer obvious (which the Applicant strongly denies) it adds no teaching whatsoever regarding the relationship between the thickness of the first layer and the target depth.

The combination of Yao et al. and the combined teachings of Doan and Laxman is neither proper nor provides the missing teachings. The Examiner states that the sixth step etch of Yao et al. inherently covers the current claims. However, the Applicants believe that the Examiner has failed to meet the stringent requirements of an obviousness rejection based upon inherency.

In order to establish a *prima facie* case of obviousness based on inherent properties, the Examiner must show that the undisclosed properties are not only inevitably and necessarily present, but also that the inherency of the undisclosed properties or elements is obvious to one skilled in the art. *Kloster Speedsteel AB v. Crucible Inc.*, 230 USPQ 81, 88 (Fed. Cir. 1986).

There is no teaching or suggestion in Yao et al. which would obviously indicate to one skilled in the art that the two step etch of the current claims is necessarily and inevitably the result of the teaching of Yao et al.

Moreover, not only does Yao et al. not inherently cover the current claims, Yao et al. explicitly teaches away from the methods of the current claims. Yao et al. state that their unexpected results are due to the specific combination of steps 2-5. See column 3, lines 1-10. However, the sequential steps of Yao et al. are in reverse order to the steps of the current method. In other words, Yao et al. teaches away from the claimed sequence of steps. The Applicants also point to the following differences between Yao et al. and the current claims.

Furthermore, Yao et al. performs chemical etching prior to plasma etching. This is a different principle of operation than the current claims. If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Moreover, the goal of Yao et al. is to obtain a highly smooth planarized surface. Modifying the teachings of Yao et al. to do a facet etch would render the surface distinctly non-planar and as such, would be unusable for the purpose of Yao et al. In addition, Steps 3-6 of Yao et al. etches the semiconductor device beyond the first layer. This means that the target depth of the etch of Yao et al. is greater than the depth of the first layer contrary to the language of the current claims. For the above reasons, even if, arguendo, Yao et al. were properly combinable with Doan in view of Laxman, such a combination fails to teach the steps of the current method claim. Therefore, the Examiner should reconsider and withdraw the rejections of Claims 1-10 under § 103(a).

The Examiner rejected Claims 11-21 under 35 U.S.C. § 103(a) as being unpatentable over Doan in view of Laxman and Yao et al. and further in view of Lee (USP 5,935,875). The Applicants respectfully traverse this rejection. As argued above, the combination of Doan in view of Laxman in view of Yao et al. is not proper and also fails to disclose the elements of the current claims. The above arguments are repeated herein by reference. The addition of Lee does not remedy the deficiencies in the combined teachings of Doan in view of Laxman and Yao et al. nor does it render such a combination proper. As such, this rejection is improper and the *prima facie* case fails.

No fee is believed due for the filing of this response. If a fee is due, such fee should be charged to Deposit Account 23-2053 and any necessary petition should be considered provisionally made.

Respectfully submitted,

Dated: February 24, 2003

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United States Patent **6,518,624**
Kim , et al. **February 11, 2003**

Trench-gate power semiconductor device preventing latch-up and method for fabricating the same

Abstract

A trench-gate power semiconductor device and a method for fabricating the same are provided. The trench-gate power semiconductor device includes a semiconductor substrate of a first conductivity type used as a collector region, a buffer layer of a second conductivity type formed on the semiconductor substrate, a drift region of a second conductivity type formed on the buffer layer, a base region of a first conductivity type formed on the drift region, a gate dielectric layer formed on the surface of a trench which is formed down to a predetermined depth into the drift region and surrounds the base region, a gate electrode formed on the gate dielectric layer, an emitter region of a second conductivity type contacting both the surface of the base region and an upper sidewall of the trench in the base region, the emitter region contains a first emitter region formed so as to be extended to a predetermined length along the sidewall of the trench and to be alternately arranged in the base region and a second emitter region extended to a predetermined length from the first emitter to the center of the basc region, an emitter electrode formed so as to be electrically connected to the first emitter region through a part of the second emitter region, and a collector electrode formed so as to be electrically connected to the semiconductor substrate.

Inventors: **Kim; Hyun-chul** (Shihung, KR); **Yun; Chong-man** (Seoul, KR); **Lee; Kyu-hyun** (Bucheon, KR); **Kim; Ju-il** (Bucheon, KR)

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Appl. No.: **734016**

Filed: **December 12, 2000**

Foreign Application Priority Data

May 30, 2000[KR] 00-29298

Current U.S. Class: **257/330**; 257/328; 257/331; 257/401

Intern'l Class: H01L 029/76

Field of Search: 257/328-334,401 438/268-274

References Cited [Referenced By]

U.S. Patent Documents

5072266	Dec., 1991	Bulucea et al.	357/23.
5468982	Nov., 1995	Hshieh et al.	257/331.

5545908	Aug., 1996	Tokura et al.	257/341.
5895952	Apr., 1999	Darwish et al.	257/330.
5910669	Jun., 1999	Chang et al.	257/339.
6005271	Dec., 1999	Hshieh	257/341.

Foreign Patent Documents

11-87690	Mar., 1999	JP

Primary Examiner: Loke; Steven
Assistant Examiner: Nadav; Ori
Attorney, Agent or Firm: Rothwell, Figg, Ernst & Manbeck

Claims

What is claimed is:

1. A trench-gate power semiconductor device comprising:

a semiconductor substrate of a first conductivity type used as a collector region;

a buffer layer of a second conductivity type formed on the semiconductor substrate;

a drift region of a second conductivity type formed on the buffer layer;

a base region of a first conductivity type formed on the drift region;

a gate dielectric layer formed on the surface of a trench which is formed down to a ***predetermined depth*** into the drift region and surrounds the base region;

a gate electrode formed on the gate dielectric layer;

an emitter region of a second conductivity type contacting both the surface of the base region and an upper sidewall of the trench in the base region, the emitter region contains a first emitter region formed so as to be extended to a predetermined length along the sidewall of the trench and to be alternately arranged in the base region and a second emitter region extended to a predetermined length from the first emitter to the center of the base region;

an emitter electrode formed so as to be electrically connected to the first emitter region through a part of the second emitter region;

a collector electrode formed so as to be electrically connected to the semiconductor substrate; and

a first region of a first conductivity type having a higher impurity concentration than the impurity concentration in the base region, formed so as to be overlapped with a part of the second emitter region in the base region,

wherein the first region of the first conductivity type is a square shape surrounded by the base region, and

each of the corners of the first region of the first conductivity type is extended in a circle shape toward corresponding corners of the trench.

2. The trench-gate power semiconductor device according to claim 1, wherein the base region surrounded by the trench has a square shape.

3. The trench-gate power semiconductor device according to claim 1, wherein the first conductivity type is p-type impurities, and the second conductivity type is n-type impurities.

4. A trench-gate power semiconductor device comprising:

a semiconductor substrate of a first conductivity type used as a collector region;

a buffer layer of a second conductivity type formed on the semiconductor substrate;

a drift region of a second conductivity type formed on the buffer layer;

a base region of a first conductivity type formed on the drift region;

a gate dielectric layer formed on the surface of a trench which is formed down to a ***predetermined depth*** into the drift region and surrounds the base region;

a gate electrode formed on the gate dielectric layer;

an emitter region of a second conductivity type contacting both the surface of the base region and an upper sidewall of the trench in the base region, the emitter region contains a first emitter region formed so as to be extended to a predetermined length along the sidewall of the trench and to be alternately arranged in the base region and a second emitter region extended to a predetermined length from the first emitter to the center of the base region;

an emitter electrode formed so as to be electrically connected to the first emitter region through a part of the second emitter region;

a collector electrode formed so as to be electrically connected to the semiconductor substrate; and

a first region of a first conductivity type having a higher impurity concentration than the impurity concentration in the base region, formed so as to be overlapped with a part of the second emitter region in the base region,

wherein the first region of the first conductivity type is a square shape surrounded by the base region, and

two diagonally opposite corners of the first region of the first conductivity type are extended in a circle shape toward corresponding corners of the trench, and the other diagonally opposite corners are extended to one side of the trench and are simultaneously extended to a predetermined length along the sidewall of the trench in the base region, which is arranged along the sidewall of the trench.

5. The trench-gate power semiconductor device according to claim 4, wherein the base region surrounded by the trench has a square shape.

6. The trench-gate power semiconductor device according to claim 4, wherein the first conductivity type is p-type impurities, and the second conductivity type is n-type impurities.

Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a power semiconductor device and a method for fabricating the same, and more particularly, to a trench-gate power semiconductor device preventing latch-up and a method for fabricating the same.

United States Patent **6,511,777**
Pas **January 28, 2003**

Method for manufacturing a phase shift photomask

Abstract

A method for fabricating a phase shift photomask (10) includes providing a photomask (12) having a substantially opaque layer (16) on a surface (14) of a substantially transparent substrate (18). The opaque layer (14) includes a removed portion to define a light transmitting pattern (20) of the photomask (12). The method also includes depositing an implant (22) in a portion of the substrate (18). The implanted portion (24) of the substrate (18) includes an etch rate different than an etch rate of an unimplanted portion (32) of the substrate (18). The method includes initiating an etch of the substrate (18) corresponding to the light transmitting pattern (20) and monitoring a rate of the etch. The method further includes terminating the etch in response to detecting a change in the rate of the etch.

Inventors: **Pas; Sylvia D.** (Plano, TX)
Assignee: **Texas Instruments Incorporated** (Dallas, TX)
Appl. No.: **666933**
Filed: **September 21, 2000**

Current U.S. Class: **430/5**; 216/62
Intern'l Class: G03F 009/00; C03C 015/00
Field of Search: 430/5,322,323,30 216/62,87

References Cited [Referenced By]

U.S. Patent Documents

5376483	Dec., 1994	Rolfson	430/5.
5480747	Jan., 1996	Vasudev	430/5.
5672449	Sep., 1997	Loschner et al.	430/5.
6261725	Jul., 2001	Tzu et al.	430/5.

Primary Examiner: Rosasco; S.
Attorney, Agent or Firm: Keagy; Rose Alyssa, Brady, III; W. James, Telecky, Jr.; Frederick J.

Parent Case Text

This application claims priority under 35 USC .sctn.119(e)(1) of provisional application No. 60/163,864 filed Nov. 5, 1999.

Claims

What is claimed is:

1. A method for fabricating a phase shift photo mask, comprising:

providing a photomask having a substantially opaque layer on a surface of a substantially transparent substrate, the opaque layer having a removed portion to define a light transmitting pattern of the photomask;

depositing an implant in a portion of the substrate, the implanted portion of the substrate having an etch rate different than an etch rate of an unimplanted portion of the substrate;

initiating an etch of the substrate corresponding to the light transmitting pattern;

monitoring a rate of the etch; and

terminating the etch in response to detecting a change in the rate of the etch.

2. The method of claim 1, wherein depositing the implant comprises implanting a dopant to a ***predetermined depth*** of the substrate from the surface of the substrate.

3. The method of claim 2, wherein terminating the etch comprises terminating the etch in response to detecting the etch rate of the unimplanted portion of the substrate.

4. The method of claim 1, wherein depositing the implant comprises implanting an interlayer at a ***predetermined depth*** of the substrate from the surface of the substrate.

5. The method of claim 4, further comprising:

monitoring the etch to detect the etch rate of the unimplanted portion of the substrate;

monitoring the rate of the etch to detect an etch rate of the interlayer; and

wherein terminating the etch comprises terminating the etch in response to detecting the etch rate of the unimplanted portion of the substrate after detecting the etch rate of the interlayer.

6. The method of claim 1, wherein depositing the implant comprises:

implanting a dopant to a ***predetermined depth*** of the substrate from the surface of the substrate, wherein the etch rate of the implanted portion of the substrate is greater than the etch rate of the unimplanted portion of the substrate; and

wherein terminating the etch comprises terminating the etch in response to detecting an etch rate less than the etch rate of the implanted portion of the substrate.

7. The method of claim 1, wherein depositing the implant comprises implanting an interlayer in the substrate, the interlayer disposed a predetermined distance from the surface of the substrate, the interlayer having a substantially uniform thickness, and wherein terminating the etch comprises terminating the etch in response to detecting a change in the rate of the etch corresponding to the etch rate of the unimplanted portion of the substrate after

detecting an etch rate of the interlayer.

8. A method for fabricating a phase shift photomask, comprising:

providing a photomask having a substantially opaque layer on a surface of a substantially transparent substrate, the opaque layer having a removed portion to define a light transmitting pattern of the photomask;

implanting a dopant into a portion of the substrate corresponding to the light transmitting pattern, the doped portion of the substrate having an etch rate different than an etch rate of the undoped portion of the substrate;

initiating an etch of the substrate corresponding to the light transmitting pattern;

monitoring a rate of the etch; and

terminating the etch in response to detecting the etch rate of the undoped portion of the substrate.

9. The method of claim 8, wherein implanting the dopant comprises implanting the dopant to a ***predetermined depth*** of the substrate, the ***predetermined depth*** corresponding to a desired light phase shift.

10. The method of claim 8, wherein the etch rate of the doped portion of the substrate is greater than the etch rate of the undoped portion of the substrate, and wherein terminating the etch comprises terminating the etch in response to detecting an etch rate less than the etch rate of the doped portion.

11. The method of claim 8, wherein implanting the dopant comprises implanting the dopant to a substantially uniform depth of the substrate, the depth corresponding to a desired light phase shift.

12. The method of claim 8, wherein the etch comprises a wet etch.

13. The method of claim 8, wherein monitoring the rate of the etch comprises:

detecting the etch rate of the doped portion of the substrate; and

detecting the etch rate of the undoped portion of the substrate after detecting the etch rate of the doped portion.

14. A method for fabricating a phase shift photomask, comprising:

providing a photomask having a substantially opaque layer on a surface of a substantially transparent substrate, the opaque layer having a removed portion to define a light transmitting pattern of the photomask;

implanting an interlayer in a portion of the substrate, the implanted portion of the substrate having an etch rate different than an etch rate of an unimplanted portion of the substrate;

initiating an etch of the substrate corresponding to the light transmitting pattern;

monitoring a rate of the etch;

detecting the etch rate of the implanted portion of the substrate; and

terminating the etch in response to detecting the etch rate of the unimplanted portion of the substrate after detecting the etch rate of the implanted portion.

15. The method of claim 14, wherein implanting the interlayer comprises implanting the interlayer at a ***predetermined depth*** of the substrate, the ***predetermined depth*** corresponding to a desired light phase shift.

16. The method of claim 14, wherein implanting the interlayer comprises implanting the interlayer in the substrate, the interlayer having a substantially uniform thickness.

17. The method of claim 14, wherein the etch rate of the implanted portion of the substrate is greater than the etch rate of the unimplanted portion of the substrate, and wherein terminating the etch comprises terminating the etch in response to detecting an etch rate less than the etch rate of the implanted portion.

18. The method of claim 14, wherein implanting the interlayer comprises implanting the interlayer in the portion of the substrate corresponding to the light transmitting pattern.

19. The method of claim 14, wherein initiating the etch comprises initiating a dry etch.

20. The method of claim 14, wherein monitoring the rate of the etch further comprises detecting the etch rate of the unimplanted portion of the substrate prior to detecting the etch rate of the implanted portion of the substrate.

Description

TECHNICAL FIELD OF THE INVENTION

This invention relates in general to the field of wafer manufacturing and, more particularly, to a method for manufacturing a phase shift photomask.

BACKGROUND OF THE INVENTION

Significant advancements in the miniaturization of semiconductor integrated circuits have been made in recent years. With such advancements, a reduction in a size of circuit patterns formed on semiconductor substrates, or wafers, has been achieved. One technique for producing a circuit pattern on a wafer includes photolithography. The photolithography technique generally includes transferring a circuit pattern from a photomask onto the wafer. The photomask is generally constructed by depositing a substantially opaque layer of material on a surface of a substantially transparent substrate. Portions of the opaque layer are then removed to form the pattern to be transferred to the wafer during a light exposure step of the photolithography process.

A photomask may also be used to provide phase shifting in the photolithography process. Phase shifting generally creates positive and negative phase light interference when administering the light exposure step in the photolithography process. Exposure light reaching an unexposed region of the wafer due to optical diffraction is generally canceled out by light reaching the exposed regions of the wafer because the light transmitted through the phase shift portion of the photomask is opposite in phase. Thus, phase shifting generally provides increased resolution of transferred patterns projected onto the wafer.

Forming a photomask for use with phase shift photolithography processing generally requires reducing a thickness of the light transmitting portion of the photomask substrate to produce a desired light phase shift. Reducing the thickness of the light transmitting portion of the photomask substrate may be accomplished by etching or other suitable processes. For example, the light transmitting portion of the photomask substrate may be chemically etched until a desired thickness of the photomask substrate is obtained to produce the desired light phase shift.

However, prior methods for manufacturing a phase shift photomask suffer several disadvantages. For example, variations in etching operations generally result in imprecise thicknesses of the light transmitting portions of the photomask substrate. For example, variations in the time, temperature, RF power, and other etch process variables are generally difficult to monitor and control. Thus, the resulting light phase shift often varies from the desired light phase shift due to a deviation between the obtained photomask substrate thickness and the desired photomask substrate thickness.

SUMMARY OF THE INVENTION

United States Patent **6,225,234**
Miller , et al. **May 1, 2001**

In situ and ex situ hardmask process for STI with oxide collar application

Abstract

A method or process for etching a trench in an IC structure is disclosed. The IC structure might be comprised of a plurality of different component materials arranged proximate to one another, all of which need to be etched down to a target level. A first etching chemistry is applied which preferentially etches a one type of component material. A second etching chemistry is applied which preferentially etches another type of component material. The method or process toggles back and forth between the etching chemistries until the target level is reached. The toggling techniques serves to maintain the profiles of the different component materials. One component material might also be embedded, as a collar or otherwise, around another component material. The toggling technique can serve to modulate the height, level, or shape of one material relative to another material. The toggling steps can be performed in situ or ex situ. The toggling technique can be used with different mask materials, including a photoresist or a hardmask over the IC structure.

Inventors: **Miller; Alan J.** (Moraga, CA); **Soesilo; Fandayani** (Fremont, CA)
Assignee: **Lam Research Corporation** (Fremont, CA)
Appl. No.: **539293**
Filed: **March 30, 2000**

Current U.S. Class: **438/734**; 438/735; 438/737; 438/738
Intern'l Class: H01L 021/461
Field of Search: 438/734,735,737,738

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U.S. Patent Documents

5958801	Sep., 2000	Langley	438/738.
6037266	Mar., 2000	Tao et al.	438/738.
6083845	Jul., 2000	Yang et al.	438/734.
6121098	Sep., 2000	Srobl	438/734.

Primary Examiner: Dang; Trung
Attorney, Agent or Firm: Beyer Weaver & Thomas, LLP

Claims

What is claimed is:

1. A method for etching a portion of an integrated circuit (IC) structure down to a certain ***target depth,*** the structure having a first component material area, and at least a second component material area arranged proximate to the first component material area, the method comprising:

(i) applying a first type of etching chemistry which preferentially etches the first component material area;

(ii) applying a second type of etching chemistry which preferentially etches the second component material area; and

repeating steps (i) and (ii) until the certain ***target depth*** is achieved, wherein certain profiles of the IC structure and its component material areas are maintained by toggling back and forth between the etching chemistries.

2. The method of claim 1, wherein etching a portion of an IC structure includes the formation of shallow trench isolation (STI) features.

3. The method of claim 1, wherein the first type of etching chemistry and second type of etching chemistry are applied in situ.

4. The method of claim 1, wherein the second component material area is embedded within the first component material area.

5. The method of claim 4, wherein a portion of the second component material area is modulated in height relative to the first component material area via toggling back and forth between the etching chemistries.

6. The method of claim 5, wherein the IC structure is a memory device, with the first component material area including at least a poly-silicon portion of material and a crystalline silicon portion of material and the second component material area including at least silicon oxide material.

7. The method of claim 5, wherein the memory device is a DRAM having deep trench capacitors.

8. The method of claim 6, wherein the second component material area is in the shape of a collar surrounding the poly-silicon material portion of material, whereby the toggling back and forth between the etching chemistries maintains the profile of the collar.

9. The method of claim 1, wherein the first type of etching chemistry preferentially etches crystalline or amorphous silicon materials.

10. The method of claim 9, wherein the materials include poly and single crystalline silicon materials.

11. The method of claim 10, wherein the first type of etching chemistry includes a mixture of Cl2 and HBr.

12. The method of claim 11, wherein the preferred ratio of Cl2-to-HBr is approximately 1-to-3.

13. The method of claim 9, wherein the second type of etching chemistry preferentially etches oxide materials.

14. The method of claim 13, wherein the second type of chemistry includes a mixture of CF4 and CHF3.

15. The method of claim 14, wherein the preferred ratio of CF4-to-CHF3 is approximately 3-to-1.

16. The method of claim 1, wherein the etching steps are used in association with a photoresist mask over at least a portion of the IC structure.

17. The method of claim 1, wherein the etching steps are used in association with a hard mask over at least a portion of the IC structure.

18. A process for etching to a target level a portion of an integrated circuit (IC) structure comprised of a plurality of different types of component materials, the process comprising:

(i) applying an etching chemistry to preferentially etch certain types of the plurality of component materials;

(ii) applying an etching chemistry to preferentially etch certain remaining other types of the plurality of component materials;

repeating steps (i) and (ii) until the target level is achieved, wherein certain profiles of the IC structure and its component material areas are maintained by toggling back and forth between the etching chemistries.

19. The process of claim 18, wherein the process of etching to a target level a portion of an IC structure includes the formation of shallow trench isolation (STI) features.

20. The process of claim 18, wherein different etching chemistries are applied in situ.

21. The process of claim 19, wherein one type of component material is embedded within another type of component material.

22. The process of claim 17, wherein one type of component material is modulated in height relative to another type of component material via toggling back and forth between the etching chemistries.

23. The process of claim 22, wherein the IC structure is a memory device with a first type of component material including at least a poly-silicon portion of material and a crystalline silicon portion of material and a second type of component material area including at least silicon oxide material.

24. The process of claim 23, wherein the memory device is a DRAM having deep trench capacitors.

25. The process of claim 23, wherein the second type of component material is in the shape of a collar surrounding the poly-silicon material portion of material, whereby the toggling back and forth between the etching chemistries maintains the profile of the collar.

26. The process of claim 18, wherein the etching chemistry in step (i) preferentially etches crystalline or amorphous silicon materials.

27. The process of claim 26, wherein the materials include poly and single crystalline silicon materials.

28. The process of claim 26, wherein the etching chemistry in step (i) includes a mixture of Cl2 and HBr.

29. The process of claim 28, wherein the preferred ratio of C12-to-HBr is approximately 1-to-3.

30. The process of claim 26, wherein the etching chemistry in step (ii) preferentially etches oxide materials.

31. The process of claim 30, wherein the etching chemistry in step (ii) includes a mixture of CF4 and CHF3.

32. The process of claim 31, wherein the preferred ratio of CF4-to-CHF3 is approximately 3-to-1.

33. The method of claim 18, wherein the etching steps are used in association with a photoresist mask over at least a portion of the IC structure.

34. The method of claim 18, wherein the etching steps are used in association with a hard mask over at least a portion of the IC structure.

Description

BACKGROUND OF THE INVENTION

The present invention relates to the fabrication of semiconductor integrated circuits (IC's). More particularly, the present invention relates to a process or method for controlled etching through an IC structure which has two or more materials arranged together, and where the height of one of the materials may need to be modulated relative to the other materials.

During the manufacture of a semiconductor-based product, for example, a flat panel display or an integrated circuit such as a memory cell, multiple deposition and/or etching steps may be employed. By way of example, one method of etching is plasma etching. In plasma etching, a plasma is formed from the ionization and dissociation of process gases. The positively charged ions are accelerated towards the substrate where they, in combination with neutral species, drive the etching reactions. In this manner, etched features such as vias, contacts, or trenches may be formed in the layers of the substrate.

Recently, shallow trench isolation (STI) has grown in popularity as a preferred method for forming a trench that can, among other applications, electrically isolate individual transistors in an integrated circuit. Electrical isolation is needed to prevent current leakage between two adjacent devices (e.g., transistors). Broadly speaking, conventional methods of producing a shallow trench isolation feature include: forming a hard mask over the targeted trench layer, patterning a soft mask over the hard mask, etching the hard mask through the soft mask to form a patterned hard mask, and thereafter etching the targeted trench layer to form the shallow trench isolation feature. Subsequently, the soft mask is removed (e.g., stripped) and the shallow trench isolation feature is back-filled with a dielectric material.

FIGS. 1A-1C are cross sectional views of the conventional process steps that maybe used to form shallow trench isolation features. Referring initially to FIG. 1A, there is shown a typical layer stack 10 that is part of a substrate or semiconductor wafer (not drawn to scale for ease of illustration). A silicon layer 12 is located at the bottom of layer stack 10. A pad oxide layer 14 is formed above silicon layer 12 and a nitride layer 16 is formed above pad oxide layer 14. In most situations, the pad oxide layer is used as the interlayer that is disposed between the nitride layer and the silicon layer. Furthermore, in order to create a patterned hard mask with pad oxide layer 14 and nitride layer 16, a photoresist layer 18 is deposited and patterned using a conventional photolithography step over nitride layer 16. After patterning, soft mask openings 20 (narrow) and 22 (wide) are created in photoresist layer 18 to facilitate subsequent etching. The above-described layers and features, as well as the processes involved in their creation, are well known to those skilled in the art.

Following the formation of layer stack 10, nitride layer 16 and pad oxide 14 are subsequently etched to create a hard mask, which includes a narrow hard mask opening 24 and a wide hard mask opening 26, as seen in FIG. 1B. The hard mask openings are used to pattern the trench during etching of the silicon layer. For the most part, etching stops after reaching silicon layer 12, however, a small portion 28 on the surface of silicon layer 12 is typically etched away during the etching of pad oxide layer 14. Moreover, a gas chemistry that includes CF4 is generally used to facilitate etching through the nitride and pad oxide layers. Typically, the CF4 chemistry etches the side walls of nitride layer 16, pad oxide layer 14 and small portion 28 of silicon layer 12 anisotropically (i.e., substantially straight down).

Once hard mask openings are created through nitride layer 16 and pad oxide layer 14, silicon layer 12 is etched therethrough to form shallow trench isolation features, for example, a narrow feature 30 and a wide feature 32, as